

Fig 1

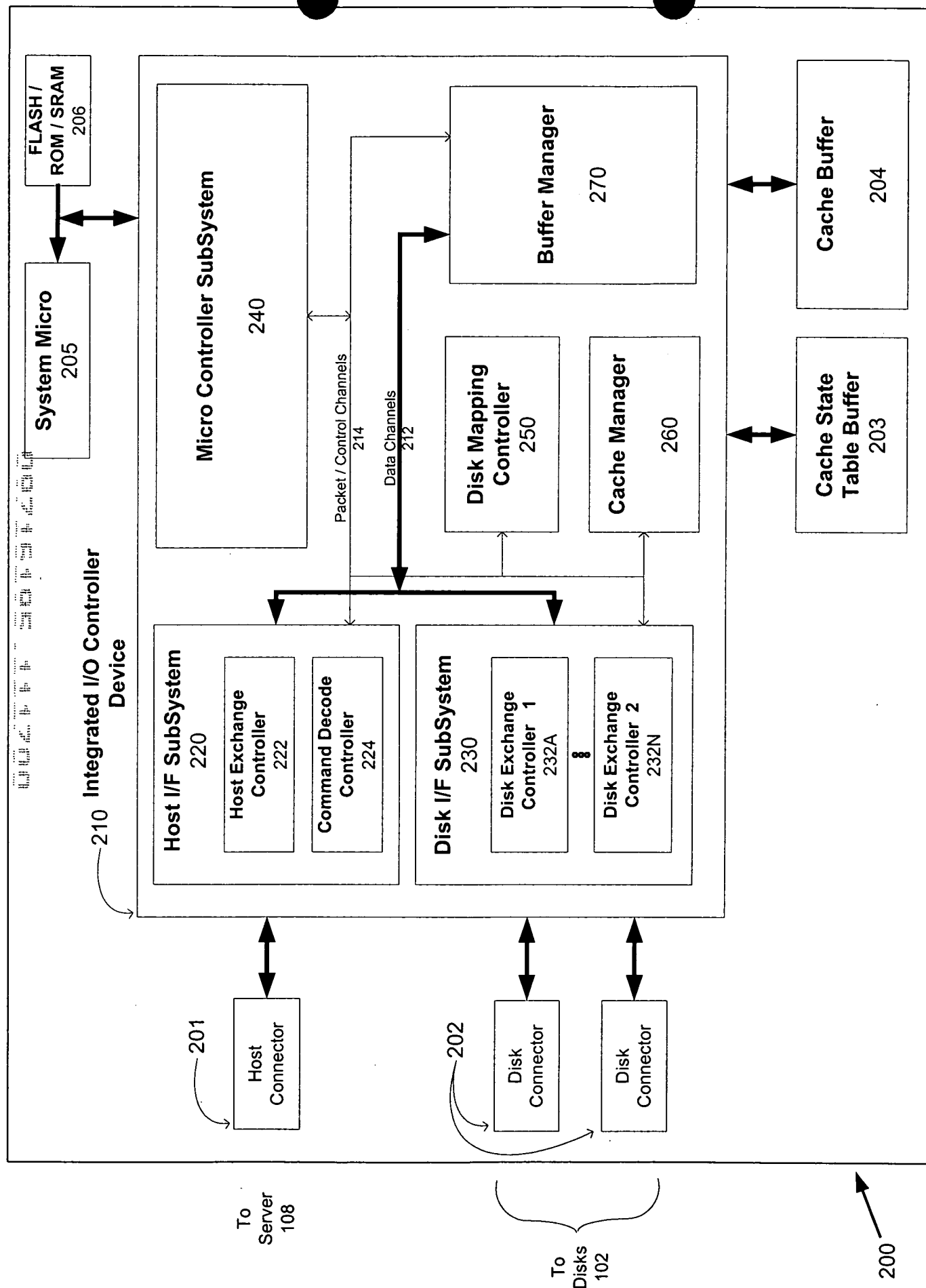


Fig 2 Integrated I/O Controller PCBA Diagram

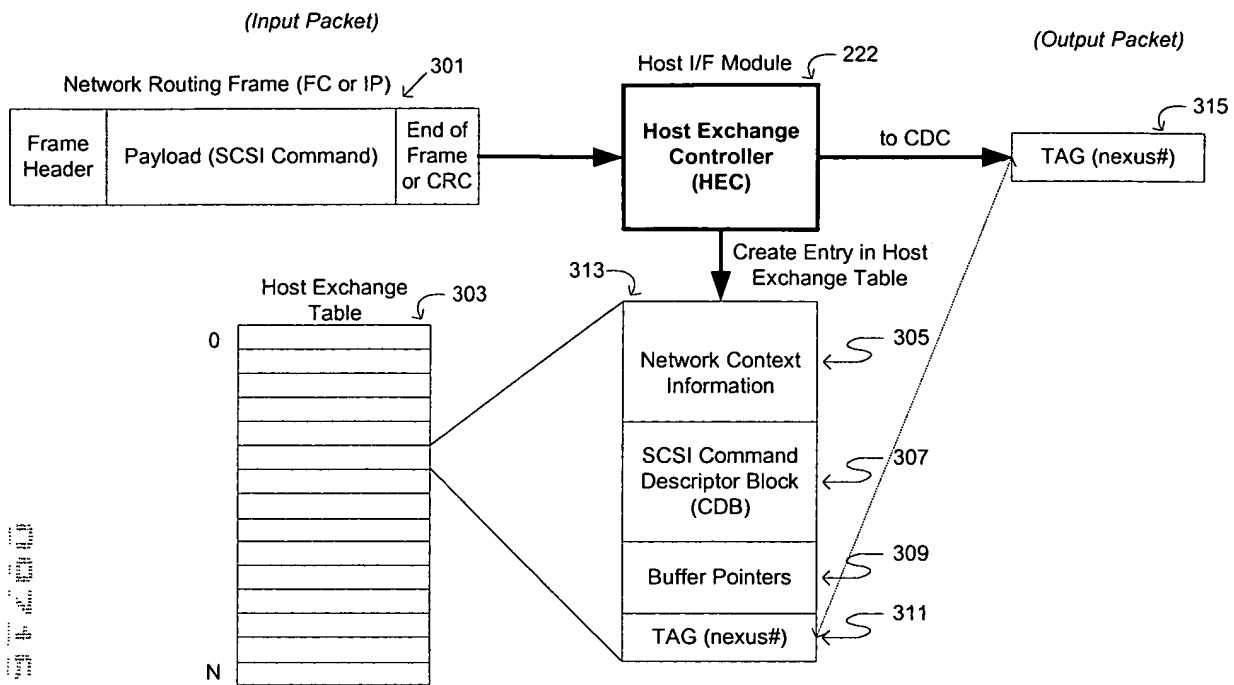


fig 3

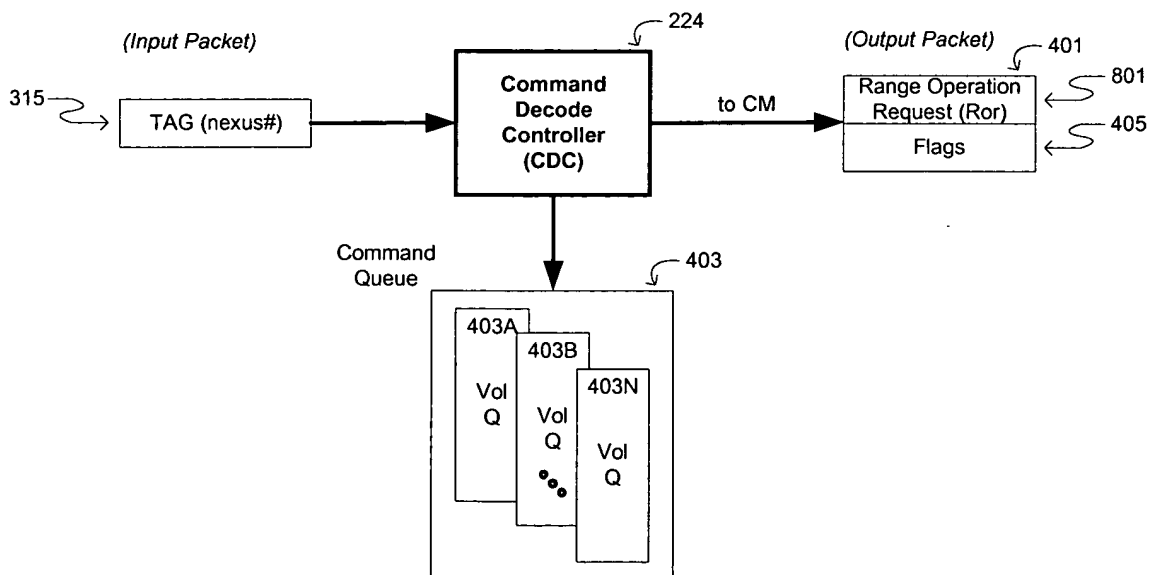


fig 4

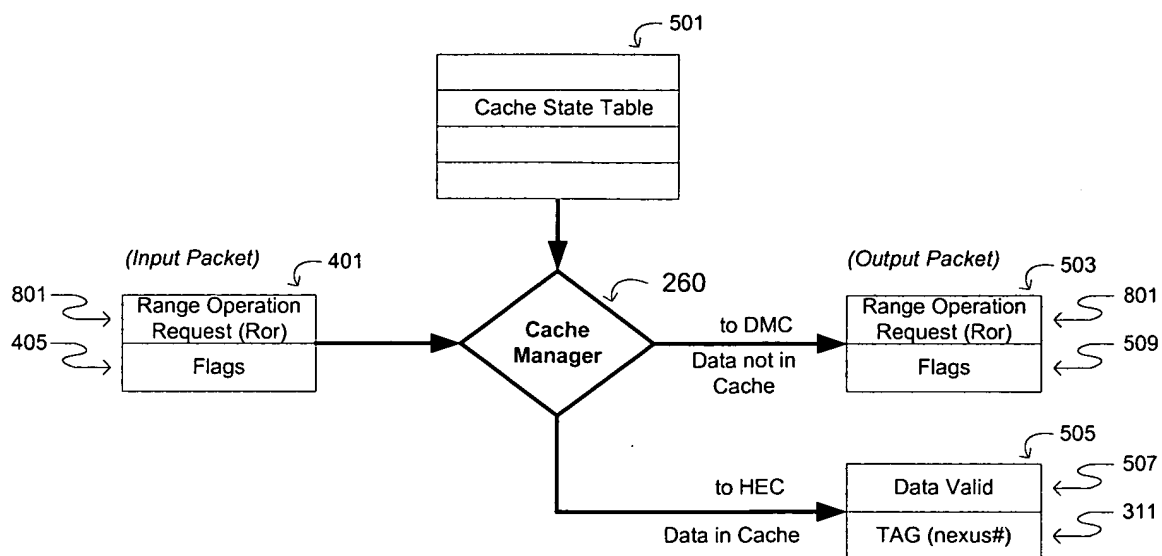


fig 5

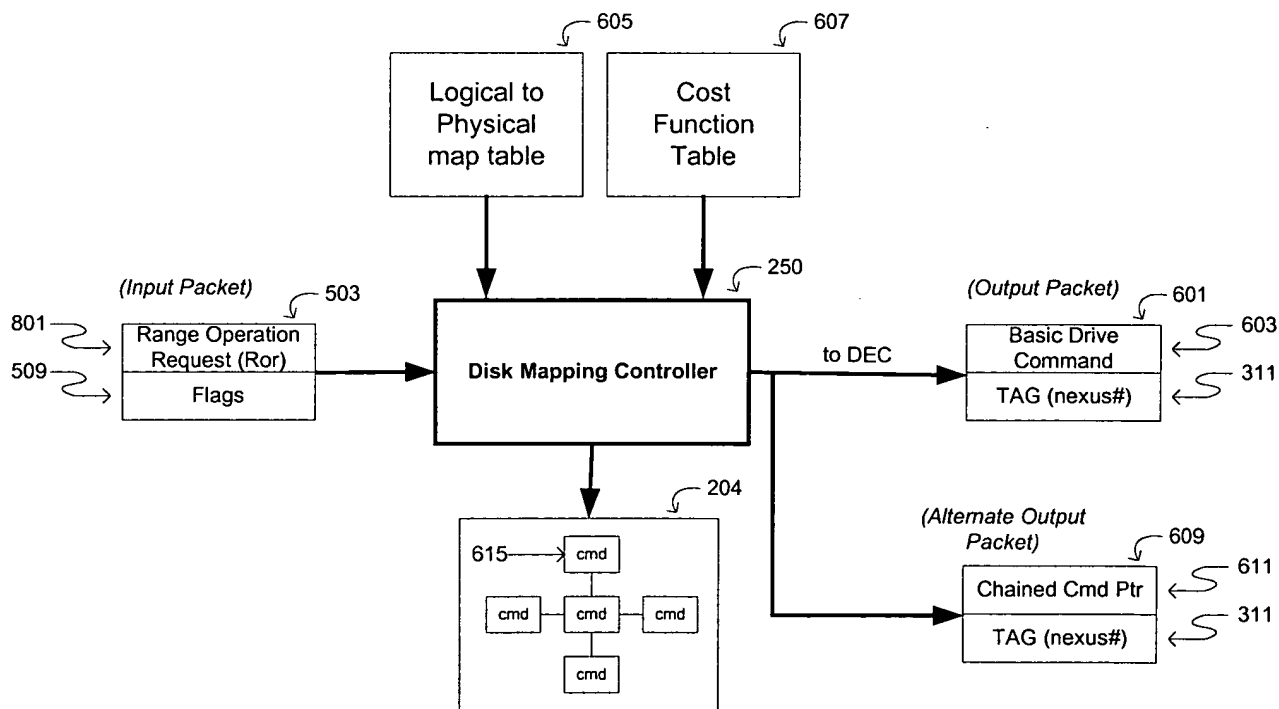


fig 6

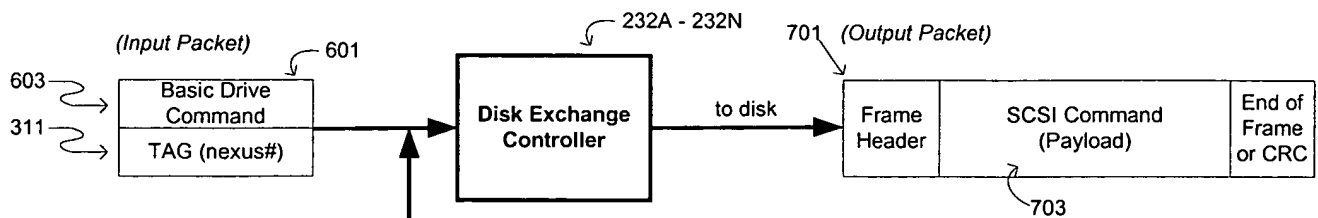


fig 7

Range Operation Request (Ror) packet

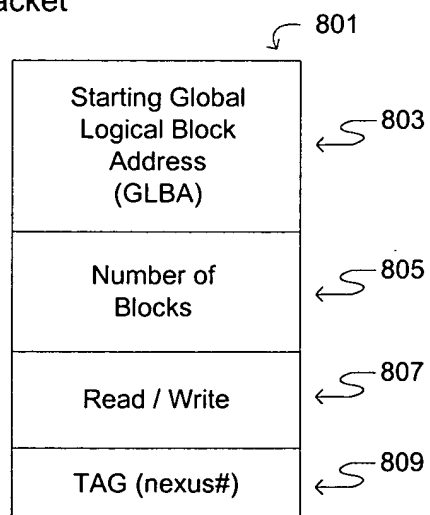


fig 8

Host Read
Command Flow

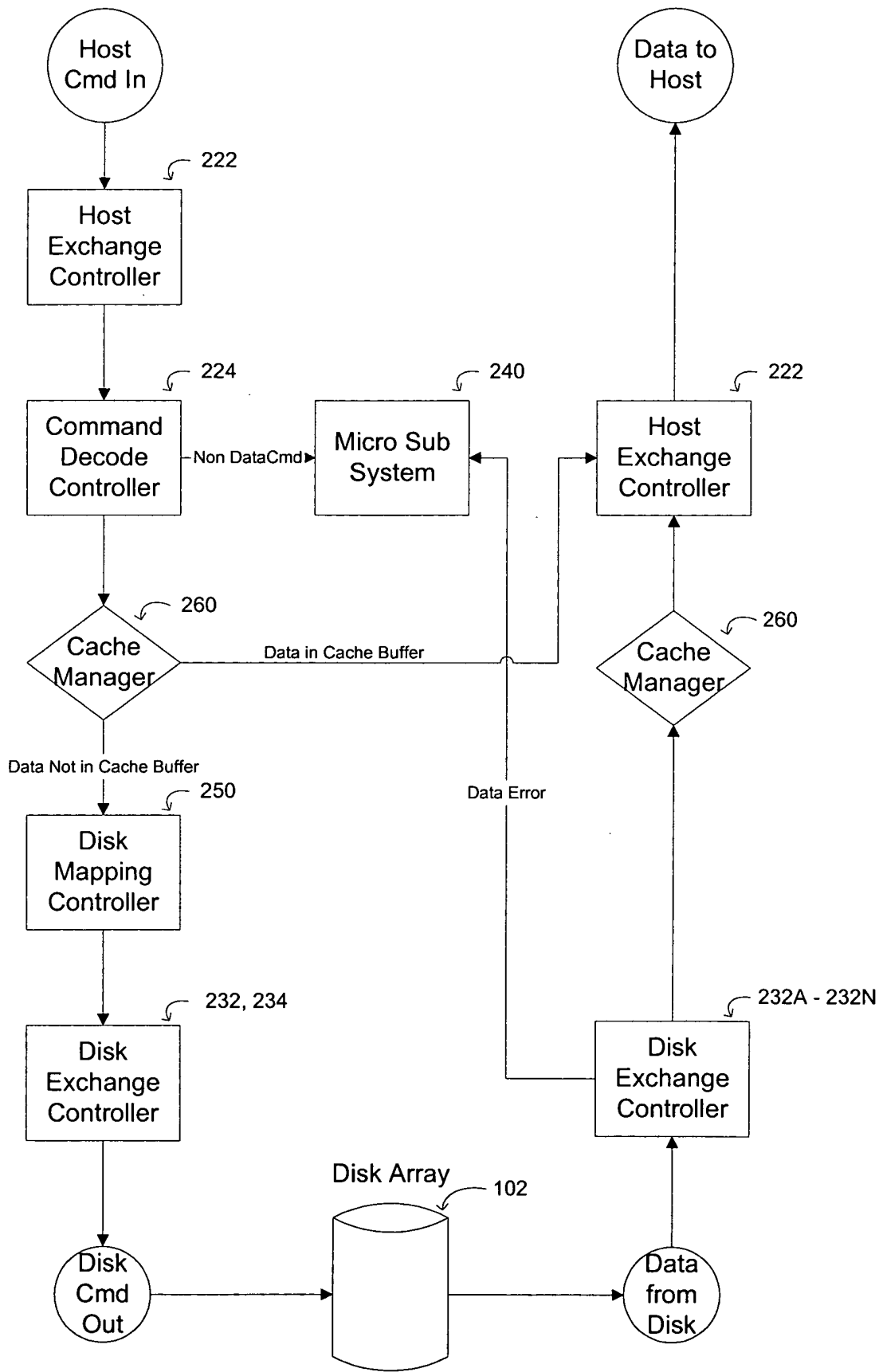


fig 9

Host Write Command Flow

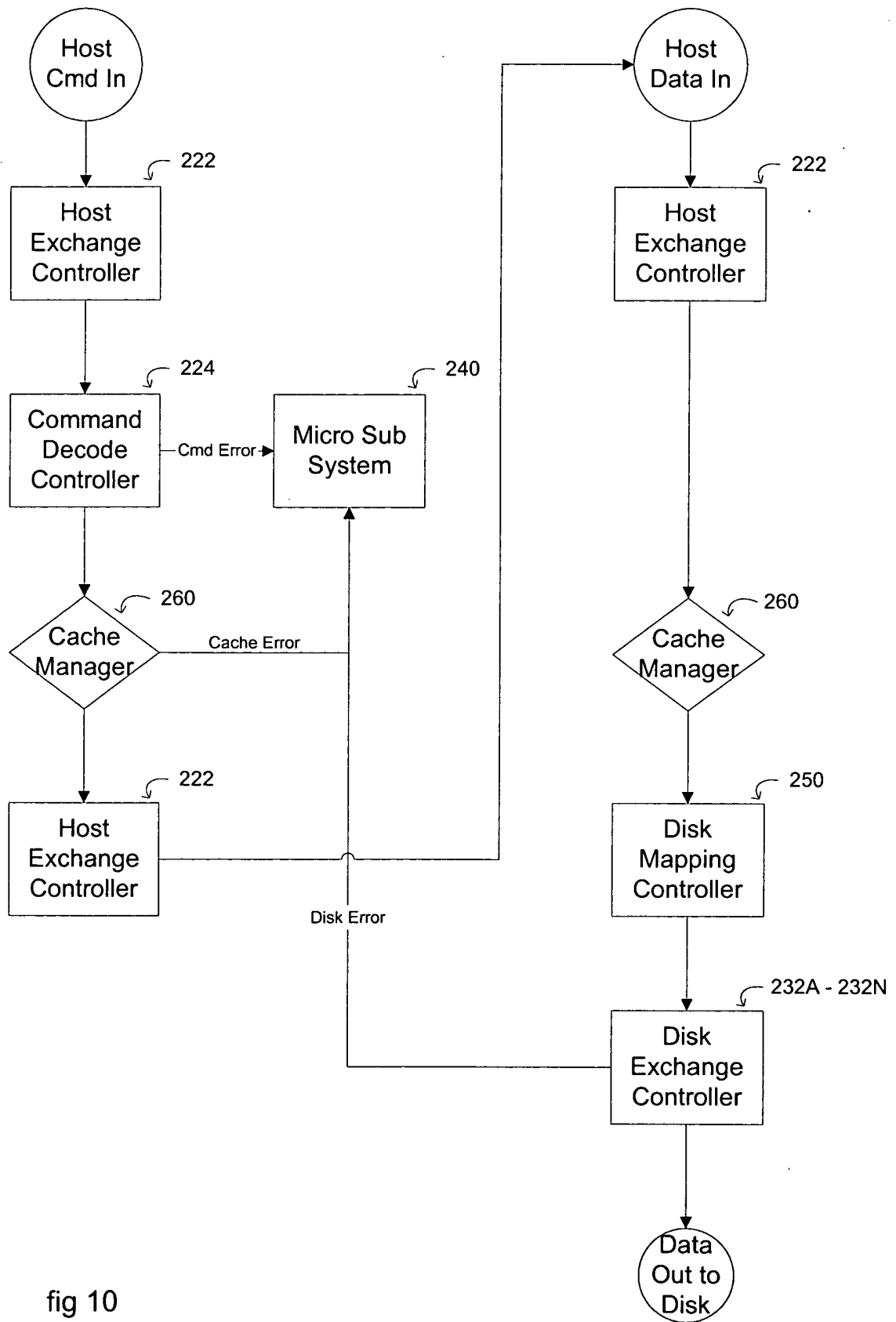


fig 10

to Disk array 102